What is claimed:

1. Method for providing a plurality of aligned instructions from an instruction stream provided by a memory unit for execution within a pipelined microprocessor comprising a prefetch buffer, whereby said prefetch buffer stores prefetched instructions and additional information about the validity and size of said prefetch buffer, said method comprising the steps of:

- in case said prefetch buffer containing invalid data:

a) requesting an instruction stream and storing said instruction stream in said prefetch buffer;

b) setting said data for validity in said prefetch buffer;

c) issuing a requested number of instructions from said requested instruction stream;

d) depending on how many instructions are issued, reducing the size data in said prefetch buffer, respectively; and

e) invalidating said validity data if all instructions from said prefetch buffer have been issued; and

- in case said prefetch buffer contains valid data:

f) issuing a requested number of instructions from said prefetch buffer;

g) depending on how many instructions are issued, reducing the data for the number of instructions stored in said prefetch buffer, respectively;

h) invalidating said validity data if all instructions from said prefetch buffer have been issued;

2. Method according to claim 1, wherein if in step f) the number of stored instructions is less than the number of requested instructions,

requesting a further instruction stream from said memory unit and combining the necessary instructions from said further instruction stream with the prefetched instructions.

3. Method for providing a plurality of aligned instructions from an instruction stream provided by a memory unit for execution within a pipelined microprocessor comprising a first and second prefetch buffer, whereby said prefetch buffers store prefetched instructions and additional information about the validity and size of said prefetch buffers, said method comprising the steps of:

- in case both of said prefetch buffers contain invalid data:

a) requesting an instruction stream and storing said instruction stream in said first prefetch buffer;

b) setting said data for validity in said first prefetch buffer;

c) issuing a requested number of instructions from said requested instruction stream;

d) depending on how many instructions are issued, reducing the size data in said first prefetch buffer;

e) invalidating said validity data if all instructions from said first prefetch buffer have been issued;

- in case one or both of said prefetch buffers contains valid data:

f) issuing a requested number of instructions from said one prefetch buffer;

g) depending on how many instructions are issued, reducing the size data in said one prefetch buffer;

h) invalidating said validity data if all instructions from said one prefetch buffer have been issued.

4. Method according to claim 3, wherein if in step f) the number of stored instructions is less than the number of requested instructions, combining the necessary instructions from said other prefetch buffer with the prefetched instructions from said one prefetch buffer.

5. Method according to claim 3, wherein before step f) the following steps are inserted:

e1) requesting an instruction stream and storing said instruction stream in the respective other prefetch buffer;

e2) setting said data for validity in said other prefetch buffer;

6. Method according to claim 3, wherein in step g) additional information will be set in both prefetch buffers indicating which prefetch buffer contains older instructions with respect to an instruction sequence.

7. Method according to claim 3, comprising after step f) in case of one prefetch buffer containing invalid data the step of requesting an instruction stream and storing said instruction stream in the respective other prefetch buffer.

8. Method according to claim 3 comprising after step c) the step of requesting an instruction stream and storing said instruction stream in the respective other prefetch buffer.

9. Apparatus for providing a plurality of aligned instructions from an instruction stream provided by a memory unit for execution

within a pipelined microprocessor comprising:

- a first prefetch buffer coupled with said memory unit, whereby said first prefetch buffer stores prefetched instructions and additional information about the validity and size of said first prefetch buffer,

- a first plurality of multiplexers with inputs coupled with said first prefetch buffer and said memory unit for selecting a certain number of instructions and with outputs,

- a second plurality of multiplexers with inputs coupled with said outputs of said first multiplexers for aligning said selected instructions.

10. Apparatus as in claim 9, wherein at least a second prefetch buffer coupled with said memory unit and with inputs of said first multiplexers is provided.

11. Apparatus as in claim 10, wherein said first and second prefetch buffer contain information about which one of the prefetch buffers contains older instructions.

12. Apparatus as in claim 10, further comprising a prefetch buffer control unit for selecting and read/write control of said first and second prefetch buffers and for updating said additional information in said first and second prefetch buffers.

13. Apparatus as in claim 10, wherein each instruction stream provided by said memory unit comprises at least four words containing a plurality of instructions, each prefetch buffer stores at least four words containing a plurality of instructions, and wherein the first multiplexers consist of at least four multiplexers having three inputs

and an output, respectively for selecting one of said words from one of said instruction stream or prefetch buffers, and wherein the second multiplexers consist of at least four multiplexers having four inputs and an output, respectively, for aligning said selected words from said first multiplexers.